SONY

CXP81800

CMOS 8-bit Single Chip Microcomputer

Piggyback/ evaluator type

Description

The CXP81800 is a CMOS 8-bit single chip micro-computer of piggyback/evaluator combined type, which is developed for evaluating the function of the CXP81840A/81848A.

100 pin PQFP (Ceramic)

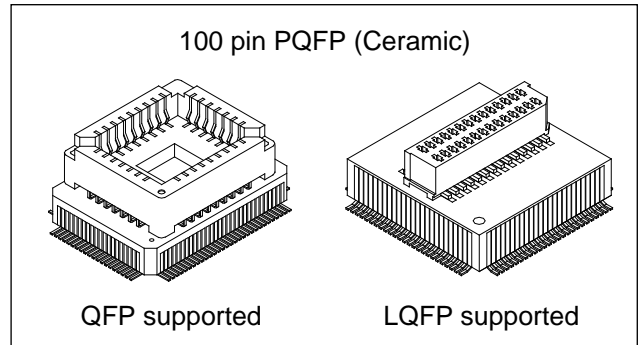QFP supported   LQFP supported

Features

• A wide instruction set (213 instructions) which cover various types of data
  – 16-bit operation/multiplication and division/ boolean bit operation instructions

• Minimum instruction cycle   333ns at 12MHz operation (3.0 to 5.5V)
                                      250ns at 16MHz operation (4.5 to 5.5V)
                                      122µs at 32kHz operation

• Applicable EPROM   LCC type 27C256, LCC type 27C512
                            (Maximum 48Kbytes are available)

• Incorporated RAM capacity   1344bytes

• Peripheral functions
  – A/D converter   8-bit, 12-channel, successive approximation method
                                           (Conversion time of 20µs/16MHz)
  – Serial interface   Incorporated 8-bit, 8-stage FIFO
                                           (auto transfer for 1 to 8bytes), 1-channel
                                           8-bit clock synchronous 1-channel
  – Timer   8-bit timer
                                           8-bit timer/counter
                                           19-bit time base timer
                                           32kHz timer/counter
  – High precision timing pattern generator   PPG 19-pin, 32-stage programmable
                                           RTG 5-pin, 2-channel
  – PWM/DA gate output   PWM output 12-bit, 2-channel
                                           (repetitive frequency 62.5kHz/16MHz)
                                           DA gate pulse output 12-bit, 4-channel
  – FRC capture unit   Incorporated 26-bit and 8-stage FIFO
  – PWM output   14-bit, 1-channel
  – Remote control receiving circuit   8-bit pulse measuring counter 6-stage FIFO
• Interruption   21 factors, 15 vectors, multi-interruption possible
• Standby mode   SLEEP/STOP
• Package   100-pin ceramic PQFP

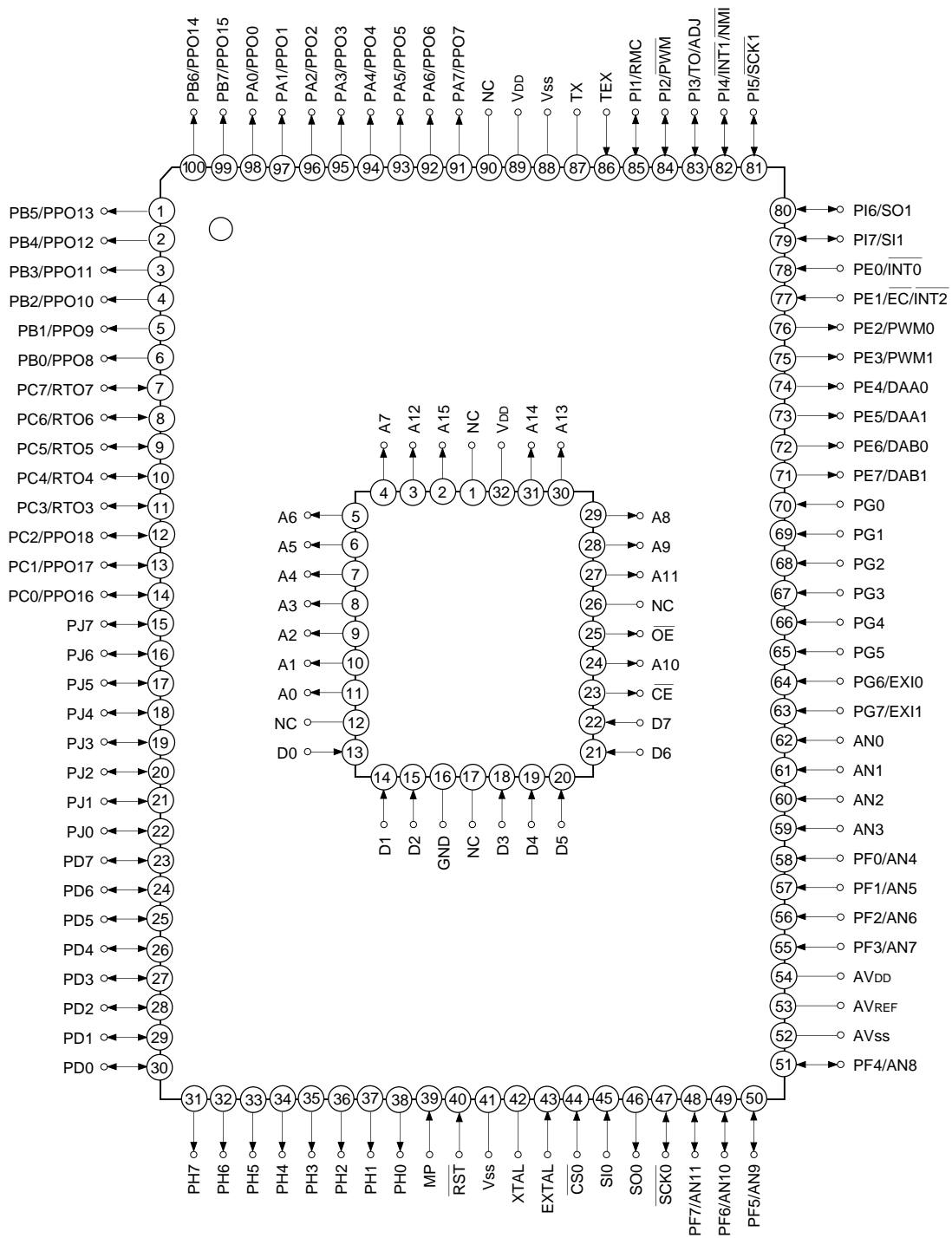**Note)** Mask option depends on the type of the CXP81800. Refer to the Products List for details.

Structure

Silicon gate CMOS IC

E95827A68-PS

Pin Configuration in Piggyback Mode (QFP package)

Top row (pins 100–81):
PB6/PPO14 (100), PB7/PPO15 (99), PA0/PPO0 (98), PA1/PPO1 (97), PA2/PPO2 (96), PA3/PPO3 (95), PA4/PPO4 (94), PA5/PPO5 (93), PA6/PPO6 (92), PA7/PPO7 (91), NC (90), VDD (89), Vss (88), TX (87), TEX (86), PI1/RMC (85), PI2/PWM (84), PI3/TO/ADJ (83), PI4/INT1/NMI (82), PI5/SCK1 (81)

Left column (pins 1–30):
PB5/PPO13 (1), PB4/PPO12 (2), PB3/PPO11 (3), PB2/PPO10 (4), PB1/PPO9 (5), PB0/PPO8 (6), PC7/RTO7 (7), PC6/RTO6 (8), PC5/RTO5 (9), PC4/RTO4 (10), PC3/RTO3 (11), PC2/PPO18 (12), PC1/PPO17 (13), PC0/PPO16 (14), PJ7 (15), PJ6 (16), PJ5 (17), PJ4 (18), PJ3 (19), PJ2 (20), PJ1 (21), PJ0 (22), PD7 (23), PD6 (24), PD5 (25), PD4 (26), PD3 (27), PD2 (28), PD1 (29), PD0 (30)

Right column (pins 80–51):
PI6/SO1 (80), PI7/SI1 (79), PE0/INT0 (78), PE1/EC/INT2 (77), PE2/PWM0 (76), PE3/PWM1 (75), PE4/DAA0 (74), PE5/DAA1 (73), PE6/DAB0 (72), PE7/DAB1 (71), PG0 (70), PG1 (69), PG2 (68), PG3 (67), PG4 (66), PG5 (65), PG6/EXI0 (64), PG7/EXI1 (63), AN0 (62), AN1 (61), AN2 (60), AN3 (59), PF0/AN4 (58), PF1/AN5 (57), PF2/AN6 (56), PF3/AN7 (55), AVDD (54), AVREF (53), AVss (52), PF4/AN8 (51)

Bottom row (pins 31–50):
PH7 (31), PH6 (32), PH5 (33), PH4 (34), PH3 (35), PH2 (36), PH1 (37), PH0 (38), MP (39), RST (40), Vss (41), XTAL (42), EXTAL (43), CS0 (44), SI0 (45), SO0 (46), SCK0 (47), PF7/AN11 (48), PF6/AN10 (49), PF5/AN9 (50)

Inner package (piggyback socket):
Top: A7 (4), A12 (3), A15 (2), NC (1), VDD (32), A14 (31), A13 (30)
Left: A6 (5), A5 (6), A4 (7), A3 (8), A2 (9), A1 (10), A0 (11), NC (12), D0 (13)
Bottom: D1 (14), D2 (15), GND (16), NC (17), D3 (18), D4 (19), D5 (20)
Right: A8 (29), A9 (28), A11 (27), NC (26), OE (25), A10 (24), CE (23), D7 (22), D6 (21)
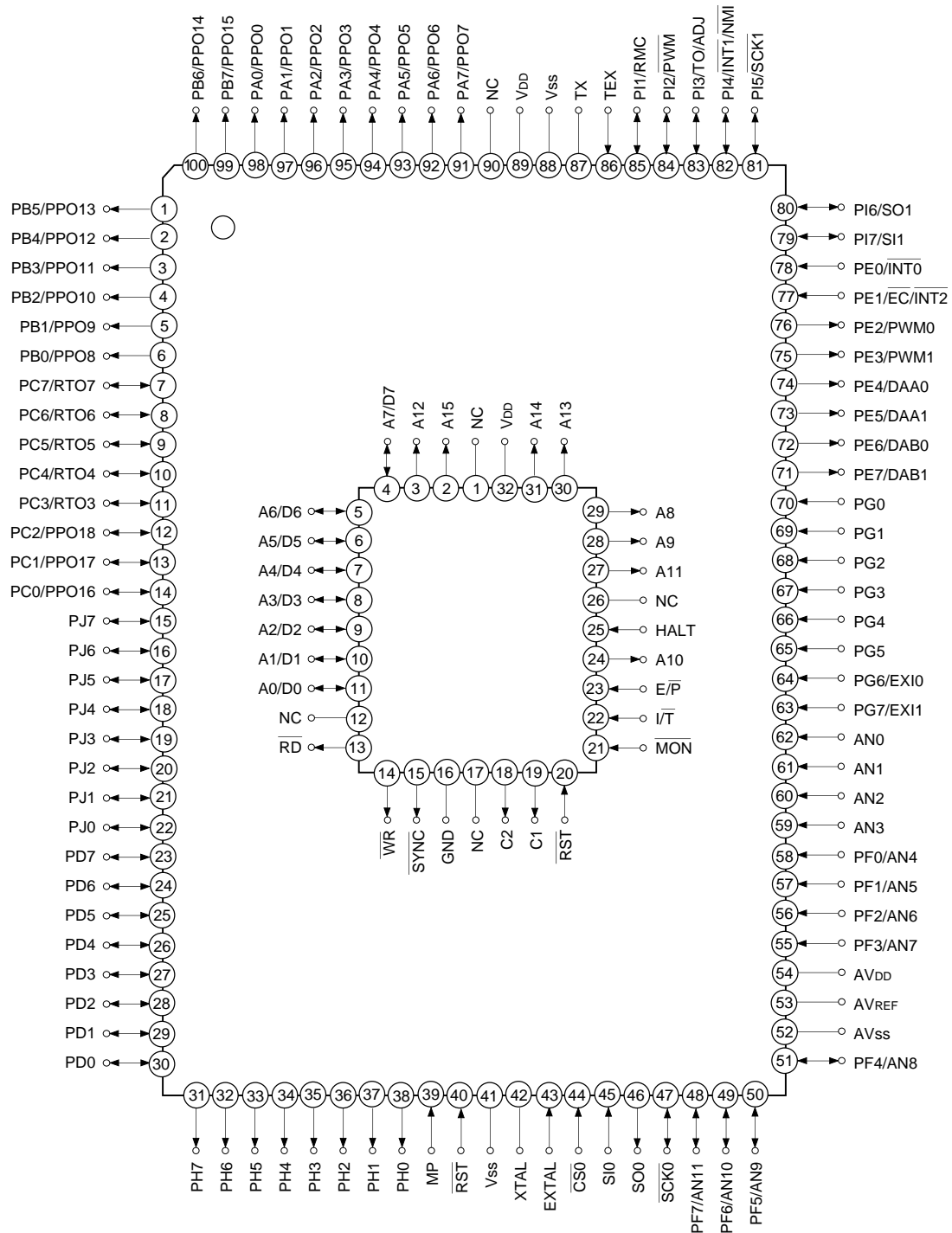
Note) 1. NC (Pin 90) is always connected to VDD.

2. Vss (Pins 41 and 88) are both connected to GND.

3. MP (Pin 39) is always connected to GND.

Pin Configuration in Piggyback Mode (LQFP package)

Top side pins (100 to 76):
PB4/PPO12 (100), PB5/PPO13 (99), PB6/PPO14 (98), PB7/PPO15 (97), PA0/PPO0 (96), PA1/PPO1 (95), PA2/PPO2 (94), PA3/PPO3 (93), PA4/PPO4 (92), PA5/PPO5 (91), PA6/PPO6 (90), PA7/PPO7 (89), NC (88), VDD (87), Vss (86), TX (85), TEX (84), PI1/RMC (83), PI2/$\overline{\text{PWM}}$ (82), PI3/TO/ADJ (81), PI4/$\overline{\text{INT1}}$/$\overline{\text{NMI}}$ (80), PI5/SCK1 (79), PI6/SO1 (78), PI7/SI1 (77), PE0/INT0 (76)

Left side pins (1 to 25):
- PB3/PPO11 (1)
- PB2/PPO10 (2)
- PB1/PPO9 (3)
- PB0/PPO8 (4)
- PC7/RTO7 (5)
- PC6/RTO6 (6)
- PC5/RTO5 (7)
- PC4/RTO4 (8)
- PC3/RTO3 (9)
- PC2/PPO18 (10)
- PC1/PPO17 (11)
- PC0/PPO16 (12)
- PJ7 (13)
- PJ6 (14)
- PJ5 (15)
- PJ4 (16)
- PJ3 (17)
- PJ2 (18)
- PJ1 (19)
- PJ0 (20)
- PD7 (21)
- PD6 (22)
- PD5 (23)
- PD4 (24)
- PD3 (25)

Right side pins (75 to 51):
- PE1/EC/$\overline{\text{INT2}}$ (75)
- PE2/PWM0 (74)
- PE3/PWM1 (73)
- PE4/DAA0 (72)
- PE5/DAA1 (71)
- PE6/DAB0 (70)
- PE7/DAB1 (69)
- PG0 (68)
- PG1 (67)
- PG2 (66)
- PG3 (65)
- PG4 (64)
- PG5 (63)
- PG6/EXI0 (62)
- PG7/EXI1 (61)
- AN0 (60)
- AN1 (59)
- AN2 (58)
- AN3 (57)
- PF0/AN4 (56)
- PF1/AN5 (55)
- PF2/AN6 (54)
- PF3/AN7 (53)
- AVDD (52)
- AVREF (51)

Bottom side pins (26 to 50):
PD2 (26), PD1 (27), PD0 (28), PH7 (29), PH6 (30), PH5 (31), PH4 (32), PH3 (33), PH2 (34), PH1 (35), PH0 (36), MP (37), $\overline{\text{RST}}$ (38), Vss (39), XTAL (40), EXTAL (41), $\overline{\text{CS0}}$ (42), SI0 (43), SO0 (44), $\overline{\text{SCK0}}$ (45), PF7/AN11 (46), PF6/AN10 (47), PF5/AN9 (48), PF4/AN8 (49), AVss (50)

Inner socket (piggyback EPROM) pinout:
- A15 (1) — VDD (28)
- A12 (2) — A14 (27)
- A7 (3) — A13 (26)
- A6 (4) — A8 (25)
- A5 (5) — A9 (24)
- A4 (6) — A11 (23)
- A3 (7) — $\overline{\text{OE}}$ (22)
- A2 (8) — A10 (21)
- A1 (9) — $\overline{\text{CE}}$ (20)
- A0 (10) — D7 (19)
- D0 (11) — D6 (18)
- D1 (12) — D5 (17)
- D2 (13) — D4 (16)
- GND (14) — D3 (15)

Note) 1. NC (Pin 88) is always connected to VDD.

2. Vss (Pins 39 and 86) are both connected to GND.

3. MP (Pin 37) is always connected to GND.

Pin Configuration in Evaluator Mode (QFP package)

Left side pins:
- PB5/PPO13 — 1
- PB4/PPO12 — 2
- PB3/PPO11 — 3
- PB2/PPO10 — 4
- PB1/PPO9 — 5
- PB0/PPO8 — 6
- PC7/RTO7 — 7
- PC6/RTO6 — 8
- PC5/RTO5 — 9
- PC4/RTO4 — 10
- PC3/RTO3 — 11
- PC2/PPO18 — 12
- PC1/PPO17 — 13
- PC0/PPO16 — 14
- PJ7 — 15
- PJ6 — 16
- PJ5 — 17
- PJ4 — 18
- PJ3 — 19
- PJ2 — 20
- PJ1 — 21
- PJ0 — 22
- PD7 — 23
- PD6 — 24
- PD5 — 25
- PD4 — 26
- PD3 — 27
- PD2 — 28
- PD1 — 29
- PD0 — 30

Top side pins (100–81):
- 100 — PB6/PPO14
- 99 — PB7/PPO15
- 98 — PA0/PPO0
- 97 — PA1/PPO1
- 96 — PA2/PPO2
- 95 — PA3/PPO3
- 94 — PA4/PPO4
- 93 — PA5/PPO5
- 92 — PA6/PPO6
- 91 — PA7/PPO7
- 90 — NC
- 89 — V$_{DD}$
- 88 — V$_{SS}$
- 87 — TX
- 86 — TEX
- 85 — PI1/RMC
- 84 — PI2/PWM
- 83 — PI3/TO/ADJ
- 82 — PI4/INT1/NMI
- 81 — PI5/SCK1

Right side pins:
- 80 — PI6/SO1
- 79 — PI7/SI1
- 78 — PE0/INT0
- 77 — PE1/EC/INT2
- 76 — PE2/PWM0
- 75 — PE3/PWM1
- 74 — PE4/DAA0
- 73 — PE5/DAA1
- 72 — PE6/DAB0
- 71 — PE7/DAB1
- 70 — PG0
- 69 — PG1
- 68 — PG2
- 67 — PG3
- 66 — PG4
- 65 — PG5
- 64 — PG6/EXI0
- 63 — PG7/EXI1
- 62 — AN0
- 61 — AN1
- 60 — AN2
- 59 — AN3
- 58 — PF0/AN4
- 57 — PF1/AN5
- 56 — PF2/AN6
- 55 — PF3/AN7
- 54 — AV$_{DD}$
- 53 — AV$_{REF}$
- 52 — AV$_{SS}$
- 51 — PF4/AN8

Bottom side pins (31–50):
- 31 — PH7
- 32 — PH6
- 33 — PH5
- 34 — PH4
- 35 — PH3
- 36 — PH2
- 37 — PH1
- 38 — PH0
- 39 — MP
- 40 — RST
- 41 — V$_{SS}$
- 42 — XTAL
- 43 — EXTAL
- 44 — CS0
- 45 — SI0
- 46 — SO0
- 47 — SCK0
- 48 — PF7/AN11
- 49 — PF6/AN10
- 50 — PF5/AN9

Inner package (32-pin):
Top pins (4–30):
- 4 — A7/D7
- 3 — A12
- 2 — A15
- 1 — NC
- 32 — V$_{DD}$
- 31 — A14
- 30 — A13

Left pins:
- 5 — A6/D6
- 6 — A5/D5
- 7 — A4/D4
- 8 — A3/D3
- 9 — A2/D2
- 10 — A1/D1
- 11 — A0/D0
- 12 — NC
- 13 — RD

Right pins:
- 29 — A8
- 28 — A9
- 27 — A11
- 26 — NC
- 25 — HALT
- 24 — A10
- 23 — E/P
- 22 — I/T
- 21 — MON

Bottom pins:
- 14 — WR
- 15 — SYNC
- 16 — GND
- 17 — NC
- 18 — C2
- 19 — C1
- 20 — RST

Note) 1. NC (Pin 90) is always connected to V$_{DD}$.

2. V$_{SS}$ (Pins 41 and 88) are both connected to GND.

3. MP (Pin 39) is always connected to GND.

Pin Configuration in Evaluator Mode (LQFP package)
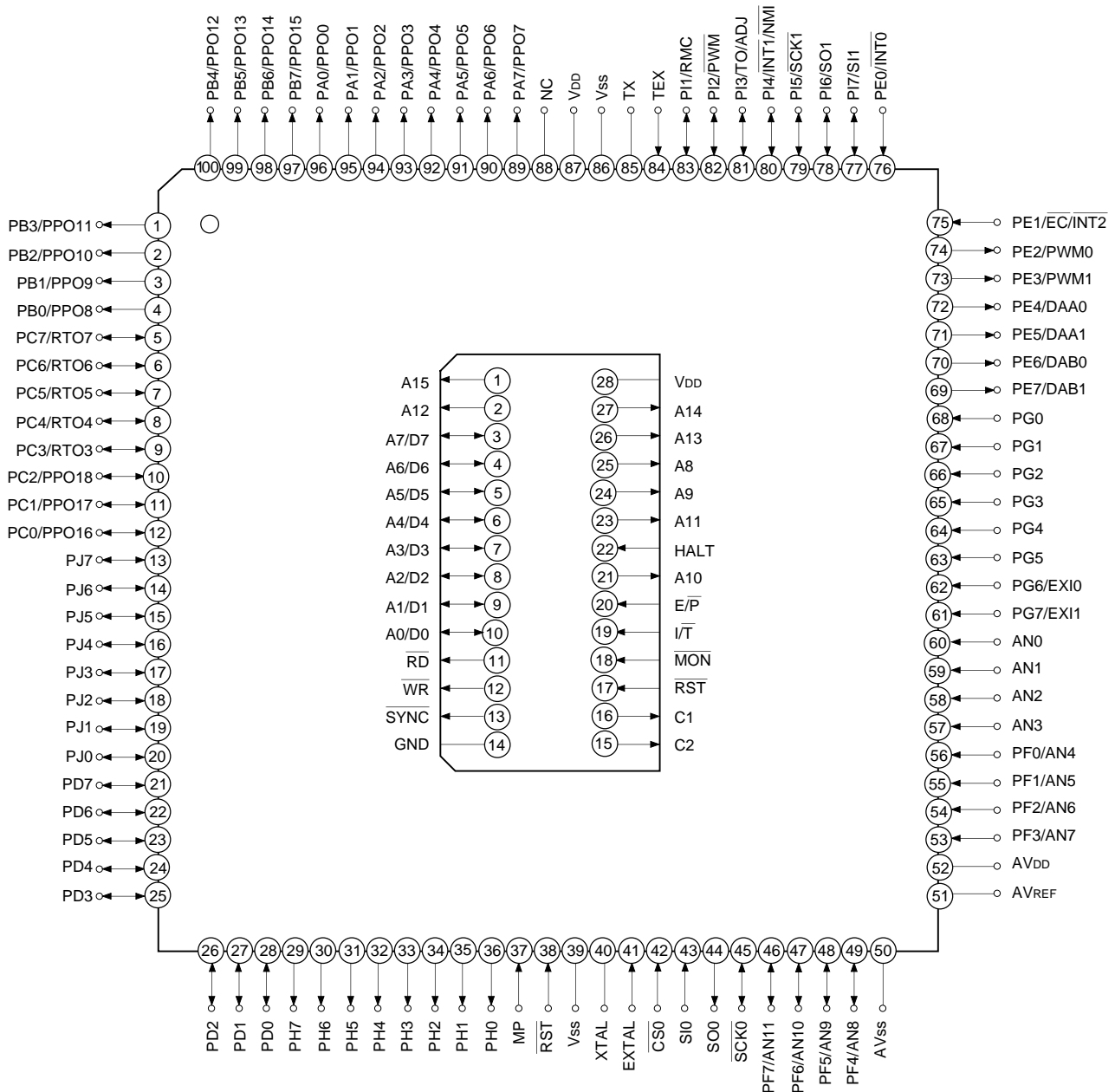
Note) 1. NC (Pin 88) is always connected to V$_{DD}$.

2. V$_{SS}$ (Pins 39 and 86) are both connected to GND.

3. MP (Pin 37) is always connected to GND.

EPROM Read Timing (Ta = −20 to +75°C, V_{DD} = 3.0 to 5.5V, Vss = 0V)

Item	Symbol	Pin	Min.	Max.	Unit
Address → data input delay time	t_{ACC}	A0 to A15 D0 to D7		100[*1] / 75[*2]	ns
Address → data hold time	t_{IH}	A0 to A15 D0 to D7	0		ns

[*1] At 12MHz operation (V_{DD} = 4.5 to 5.5V)

[*2] At 12MHz operation (V_{DD} = 3.0 to 5.5V), At 16MHz operation (V_{DD} = 4.5 to 5.5V)
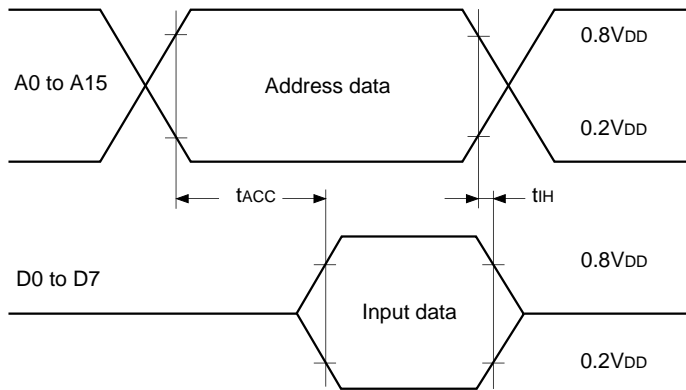
Products List

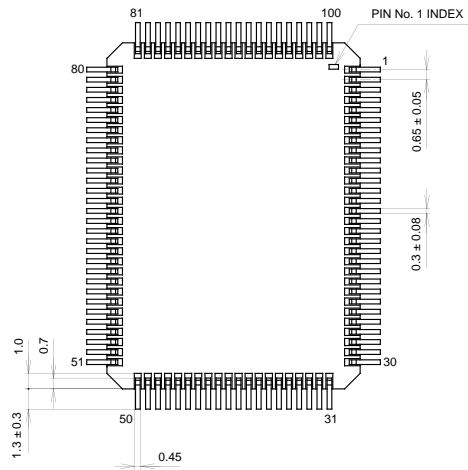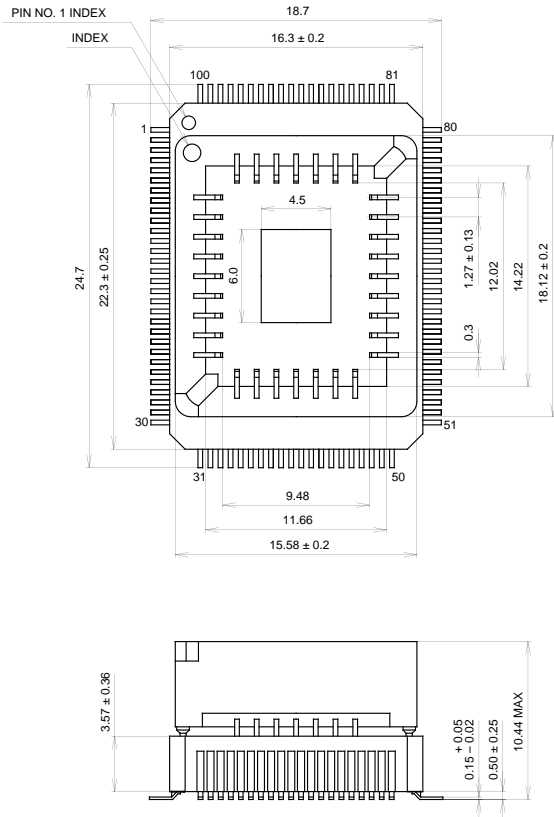| Optional item	Products			
	Mask product		Piggyback/evaluator product	
	CXP81840A	CXP81848A	CXP81800-U01Q CXP81800-U01R	CXP81800-U02R
Package	100-pin plastic QFP/LQFP		100-pin ceramic PQFP	
ROM capacitance	40Kbytes	48Kbytes	EPROM 48Kbytes	
			27C512 × 1	27C256 × 2
Pull-up resistance for reset pin	Existent/Non-existent		Existent	
Input circuit format[*1]	CMOS schmitt/TTL schmitt		TTL schmitt	CMOS schmitt

[*1] On PG4 pin and PG5 pin, the input circuit format can be selected to every pin.

Piggyback mode/evaluator mode can be switched as shown below

Piggyback mode	Piggyback/evaluator product	Evaluator mode

Pin 1 marking

LCC type EPROM
Pin 1 marking

Pin 1 index

CPU probe

(27C512 only)

Note)

Note) Evaluation cap should be
connected to CPU probe.

EPROM adaptor
Pin 1 marking

U01R used

Pin 1 index

CPU probe for LQFP

LCC type EPROM
for low voltage
Pin 1 marking

EPROM adaptor
Pin 1 marking

U02R used

For lower address   For upper address

(27C256 only)

Lower address   Upper address

Address	Memory space	EPROM (27C256)
Lower	4000H to 7FFFH	4000H to 7FFFH
Upper	8000H to FFFFH	0000H to 7FFFH

Package Outline   Unit: mm

100PIN PQFP (CERAMIC)

PIN NO. 1 INDEX
INDEX
18.7
16.3 ± 0.2
100   81
1   80
24.7
22.3 ± 0.25
4.5
6.0
1.27 ± 0.13
12.02
14.22
18.12 ± 0.2
0.3
30   51
31   50
9.48
11.66
15.58 ± 0.2

81   100   PIN No. 1 INDEX
80   1
0.65 ± 0.05
0.3 ± 0.08
1.0
0.7
51   30
1.3 ± 0.3
50   31
0.45

3.57 ± 0.36
0.15 $^{+0.05}_{-0.02}$
0.50 ± 0.25
10.44 MAX

SONY CODE	PQFP-100C-L01
EIAJ CODE	AQFP100-C-0000-A
JEDEC CODE	——————

PACKAGE STRUCTURE

PACKAGE MATERIAL	CERAMIC
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	5.7g

100PIN PQFP (CERAMIC)

□ 16.0 ± 0.4
□ 14.0 ± 0.2
75   51
76   50
0.5 ± 0.05
12.0 ± 0.15
1.5
3.2 ± 0.2
0.18 $^{+0.08}_{-0.03}$
0.8 ± 0.2
100   26
INDEX
1   25
12.8 ± 0.2

□ 12.4
0.5 ± 0.05
12.0 ± 0.15
0.18 $^{+0.08}_{-0.03}$
INDEX

3.32
0.127 $^{+0.05}_{-0.02}$
0.2 $^{+0.15}_{-0.13}$
6.9
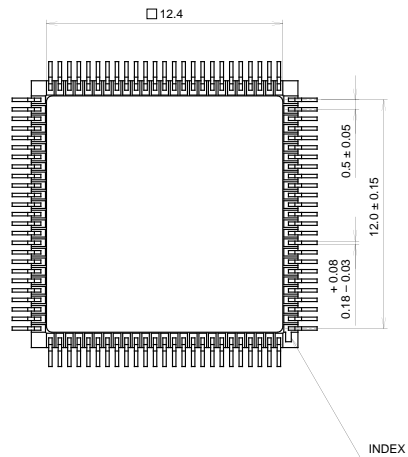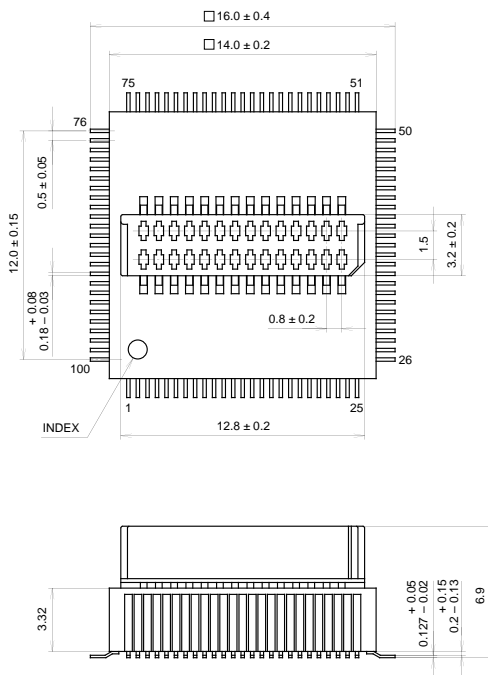
SONY CODE	PQFP-100C-L02
EIAJ CODE	AQFP100-C-1414-A
JEDEC CODE	——————

PACKAGE STRUCTURE

PACKAGE MATERIAL	CERAMIC
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	2.2g